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09/753,052	12/28/2000	Ravi Kumar Arimilli	AUS920000679US1	9307

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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	4

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/753,052	ARIMILLI ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Letter to Draftsman as received on 04/24/01; and Change of Address as received on 07/23/02.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

4. Claim 12 is rejected under 35 U.S.C. 102() as being anticipated by McCrory, U.S. Patent Number 6,513,057 (herein referred to as McCrory).

5. Referring to claim 12 McCrory has taught a multiprocessor system comprising:

a plurality of heterogenous processors with different operational characteristics and physical topology connected on a system planar (McCrory abstract figure 3, column 5 line 66-column 6 line 8);

a system bus that supports system centric operations (McCrory column 2 lines 36-67);

interrupt pins coupled to said system bus that provide connection for at least one of said plurality of heterogenous processors (McCrory column 8 lines 42-50, column 7 lines 34-43; interrupt pins would be required to communicate the interrupts to the system);

an enhanced system bus protocol that supports downward compatibility of newer processors that support advanced operational characteristics from among said plurality of processors to processors that do not support said advance operation characteristics (McCrory column 6 lines 9-65; the bus interface converter allow the different processors to communicate with each other in the system).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCrory in view of Jayakumar U.S. Patent Number 5,904,733 (herein referred to as Jayakumar).

7. Referring to claim 1 McCrory has taught a data processing system comprising:

a first processor with a first operational characteristics on a system planar and a second heterogenous processor on said system planar (McCrory column 2 lines 27-47, abstract, column 5 line 66-column 6 line 8),

wherein said interconnection means enables said first processor and said second, heterogenous processor to collectively operate as a symmetric multiprocessor (SMP) system (McCrory column 2 lines 27-47, abstract, column 5 line 66-column 6 line 8; the processors can

be from different processor families altogether, or can be from the same family can be different processor models).

McCrory has not taught having an interconnection means for later connecting a second, heterogenous processor on said system planar. Jayakumar has taught adding additional processors in an SMP environment (Jayakumar column 1 lines 10-26). Although Jayakumar has taught a traditional SMP environment, while McCrory has taught a heterogeneous SMP system, one of ordinary skill in the art at the time of the invention would recognize the benefit it adding additional processors, from different families, or from the same families of processors, to increase the resources and computing power of the system as a whole. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have an interconnection means for later connecting a second, heterogenous processor to increase the system's processing power.

8. Referring to claim 2 McCrory has taught further comprising a second, heterogenous processor connected to said system bus via said interconnect means, wherein said second, heterogenous processor is comprises more advanced s physical and operational characteristics than said first processor (McCrory column 2 lines 27-47, abstract, column 5 line 66-column 6 line 8).

9. Referring to claim 3 McCrory has taught wherein said interconnection means supports backward compatibility of said second, heterogenous processor with said first processor (McCrory column 2 lines 27-47, abstract, column 5 line 66-column 6 line 40; the processors of the same family will be backwards compatible with the other processors in the same family, the

Intel 80486 and Pentium, which are discussed would have the Pentium being backwards compatible with the 80486).

10. Referring to claim 4 McCrory has taught wherein said interconnect means is coupled to a system bus and comprises a plurality of interrupt pins for connecting additional processors to said system bus (McCrory column 6 lines 9-65).

11. Referring to claim 5 McCrory has taught further comprising an enhanced system bus protocol that enables said backward compatibility (McCrory column 2 lines 27-47, abstract, column 5 line 66-column 6 line 40; the processors of the same family will be backwards compatible with the other processors in the same family, the Intel 80486 and Pentium, which are discussed would have the Pentium being backwards compatible with the 80486 and use the bus interface converter).

12. Referring to claim 6 McCrory has taught wherein said operational characteristics includes frequency, and said second, heterogenous processor operates at a higher a frequency than said first processor (McCrory column 2 lines 27-47, abstract, column 5 line 66-column 6 line 8; the SMP includes processors from the same families, and from different families, which will be running at different clock speeds).

13. Referring to claim 7 McCrory has not explicitly taught wherein said operational characteristics includes an instruction ordering mechanism, and said first processor and second a processor utilizes a different one of a plurality of instruction ordering mechanism from among in-order processing, out-of-order processing, and robust out-of order processing.
However, McCrory has taught using heterogenous processors from different families together in a SMP system (McCrory column 2 lines 27-47, abstract, column 5 line 66-column 6 line 40).

Each card will employ a plurality of processors from the same family. And one of ordinary skill in the art would recognize that the different families of processors have different instruction execution techniques, including out-of-order techniques for instruction execution (i.e. DEC systems will not have the same ordering system as the Intel processors). And since certain families of processors would be picked by the designer for executing different types of applications, the families of processors included would simply be a design choice. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include heterogeneous processors that include different instruction ordering techniques in the different processors because the processors used would be a design choice.

14. Referring to claim 8 McCrory has not explicitly taught wherein said more advanced physical topology are from among higher number of cache levels, larger cache sizes, improved a cache hierarchy, cache intervention, and larger number of on-chip processors. However, McCrory has taught using heterogenous processors from different families together in a SMP system (McCrory column 2 lines 27-47, abstract). And since certain families of processors would be picked by the designer for executing different types of applications, the families of processors included would simply be a design choice. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include heterogeneous processors that include different cache systems and different cache sizes in the different processors because the processors used would be a design choice.

15. Referring to claim 9 McCrory has taught further comprising a switch that provides direct point-to-point connection between said first processor and later added processors (McCrory column 2 lines 27-47, abstract, column 5 line 66-column 6 line 8, figure 3; all of the processors

on separate cards are connected through the bus interface system in which they communicate with each other).

16. Referring to claim 10 McCrory has taught a method for upgrading processing capabilities of a data processing system comprising:

providing a plurality of interrupt pins from a system bus on a system planar (McCrory column 8 lines 42-50, column 7 lines 34-43; interrupt pins would be required to communicate the interrupts to the system);

enabling direct connection of a new, heterogenous processor to said system planar via said interrupt pins (McCrory column 2 lines 27-47, abstract, column 5 line 66-column 6 line 40; the processors can be from different processor families altogether, or can be from the same family can be different processor models); and

providing support for full backward compatibility by said heterogenous processor when said processor comprises more advanced operational characteristics to enable said data processing system to operate as symmetric multiprocessor system (McCrory column 2 lines 27-47, abstract, column 5 line 66-column 6 line 40; the processors of the same family will be backwards compatible with the other processors in the same family, the Intel 80486 and Pentium, which are discussed would have the Pentium being backwards compatible with the 80486). McCrory has not taught enabling direct connection of a new, heterogenous processor to said system planar via said interrupt pins. Jayakumar has taught adding additional processors in an SMP environment (Jayakumar column 1 lines 10-26). Although Jayakumar has taught a traditional SMP environment, while McCrory has taught a heterogeneous SMP system, one of ordinary skill in the art at the time of the invention would recognize the benefit it adding

additional processors, from different families, or from the same families of processors, to increase the resources and computing power of the system as a whole. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to enabling direct connection of a new, heterogenous processor to increase the system's processing power.

17. Referring to claim 11 McCrory has taught wherein said providing support includes implementing an enhanced system bus protocol to support said new, heterogenous processor (McCrory column 6 lines 9-65; the bus interface converter allow the different processors to communicate with each other in the system).

18. Referring to claim 13 McCrory has taught further comprising a switch that provides direct point-to-point connection between each of said plurality of processors and later added processors (McCrory column 2 lines 27-47, abstract, column 5 line 66-column 6 line 8, figure 3; all of the processors on separate cards are connected through the bus interface system in which they communicate with each other).

19. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCrory.

20. Referring to claim 14 McCrory has not explicitly taught wherein said plurality of processors includes heterogenous processor topologies including different cache sizes, cache states, number of cache levels, and number of processors on a single processor chip. However, McCrory has taught using heterogenous processors from different families together in a SMP system (McCrory column 2 lines 27-47, abstract). Each card will employ a plurality of processors from the same family. And since certain families of processors would be picked by the designer for executing different types of applications, the families of processors included would simply be a design choice. Therefore, it would have been obvious to one of ordinary skill

in the art at the time of the invention to include heterogeneous processors that include different cache systems and different cache sizes in the different processors because the processors used would be a design choice.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

McKenney et al., U.S. Patent Number 6,480,918, has taught a system using utilizing an SMP system for processing instructions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Examiner

Art Unit 2183

March 12, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100